3.4 A 14mW Multi-bit ΔΣ Modulator with 82dB SNR and 86dB DR for ADSL2+

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ADSL2+ is an advanced version of ADSL that can transmit at data rates up to 25Mb/s and requires an operating bandwidth of 2.2MHz. These speeds require a careful optimization of power in all the blocks used. This ΔΣM achieves the data-converter specifications for ADSL2+ with OSR of 33 and 144MHz sampling-rate. The FoM=Power/($2^{(SNDR-1.76)/6.02}\times 2\times BW$), is 0.48pJ/(conversion-step). Low-power operation is obtained by significantly reducing the voltage swing at the output of the OTAs used in the modulator. The architecture uses 10 comparators for realizing two flash ADCs, two OTAs, and some digital logic. The power consumption of the analog part is 5.1mW while that of the digital part is 8.7mW.

This circuit exploits the analog feed-forward (AFF) for reducing the output swing of the first OTA [1]. The use of AFF technique for both OTAs would enable the utilization of two single-stage OTAs, thus reducing power consumption [2]; however, the method requires performing an addition in the analog domain which necessitates an additional OTA or, for 3b or less, capacitive charge sharing at the comparator input. The used solution obtains the feed-forward action for the second OTA in the digital domain. The method requires a second flash ADC but the number of comparators does not increase.

Figure 3.4.1 shows the architecture of the system [3]. The number of bits of the two quantizers are N=4 and M=3, for the full $\pm V_{REF}$ range. The swing reduction greatly limits the operation range of the second OTA that requires only 5 comparators. As a result, the SNR is the one of a 4b ΔΣM with total of 7+5 comparators. The digital feed-forward (DFF) signal is a *3-bit* quantized version of the input signal. The additional branch at the input of the second integrator compensates for the effect of the quantization noise, E_2. The K block is intended to add to the digital output a contribution opposite to that of the DFF. Thus,

$$K(z)\frac{a_2 z^{-1}}{1-z^{-1}} = -z^{-1} \Leftrightarrow K(z) = -\frac{1-z^{-1}}{a_2} \quad (1)$$

The auxiliary ADC and DAC share the delay before the K block. Since $K(z)$ cancels the effect of quantization noise, E_2, the auxiliary ADC can use any number of bits. However, it is chosen to be a 3b ADC to optimize the area, swing, and implementation in this design. Simulation results show that, with the 3b ADC, the swing of the second OTA output is $\pm 0.32V_{REF}$. Therefore, the number of quantization levels required by the main ADC, for a 4b equivalent ADC, is 16×0.32→6. The swing at the output of the first OTA is $\pm 0.15V_{REF}$.

Figure 3.4.2 shows the SC implementation of the DFF ΔΣM where a 7-level and 5-level ADC replaces the 8-level and 6-level ADC, respectively, for further hardware optimization. The coefficients are: a_1=0.5 and a_2=2 and the system transfer function is

$$Y = \left(2z^{-1} - z^{-2}\right)X + \left(1 - z^{-1}\right)^2 E_1 \quad (2)$$

where E_1 is the quantization error of the 5-level quantizer. The signal transfer function peaking is 0.08dB at 2.2MHz. The first stage input sampling capacitors, $C_{IN11,12,13}$, also perform the 7-level DAC operation while $C_{IN14,15}$ only work as the 5-level DAC. The value of the first stage sampling capacitor is 1.8pF in total. The input of the second stage uses two arrays of capacitors: C_{IN2} made by five elements, $C_{IN21,22,23}$ for sampling the preceding stage output and the 7-level DAC and $C_{IN24,25}$ for the AFF and the 5-level DAC, and C_{AUX} made by 4 elements for the AFF and the auxiliary 7-level DAC. The input capacitance value in the second stage is 1.3pF. Behavioral simulations determine the specifications of the OTAs. The dc-gain of the OTAs are $A_{0,1}$>40dB and $A_{0,2}$>80dB; the GBW and slew-rate (SR) are GBW_1>300MHz, GBW_2>200MHz, SR_1>60V/µs, and SR_2>180V/µs. Behavioral simulations also show that, because of the first-order noise shaping, the harmonic tones are below -80dBFS even with a 5% capacitance mismatch in the auxiliary DACs of the second integrator. The circuit suppresses the above tone level with the individual level averaging (ILA) logic used separately for the 7-level DAC, and the 5-level DAC of the first and second integrator.

The alleviated OTA output swing requirements permit to use single-stage telescopic OTAs. The gain-boosting technique enhances the gain of the second OTA as shown in Fig. 3.4.3. The auxiliary amplifier A_P has a scheme with a complementary configuration. The third branch of the input stage, that is biased with V_{CN}, determines the gate voltage of $M_{A1,A2}$ and, in turn, the source voltages of $M_{M1,M2}$ [4]. The use of a scaled current through M_{A3} (also scaled) saves power. All capacitors are made by MIM structures whose linearity and accuracy is sufficient for this design. The delayed bottom-plate sampling technique minimizes the signal-dependent charge injection. Each comparator consists of a 4-input preamplifier, a regenerative latch, and set-reset flip-flop. The references of both ADCs are generated by a resistive divider. The sharing of these references minimizes the power consumption and ensures thresholds matching. The resistive divider is made by a parallel connection of interdigitized poly resistors for reducing the process variation effect. The digital filter is a simple edge-detector.

The technology used for implementing the modulator is a 1P 6M 0.18µm CMOS process, and the chip area is 2.32mm². In the analog section, the first and second OTA and the internal ADC with the resistive ladder dissipate 1.7mW, 2.2mW, and 1.2mW, respectively, and the digital part consumes 8.7mW. The relatively high power is due to a high clocking frequency and the need to use a 2.5V digital supply for having the logic blocks work properly. An optimization of the digital design would reduce the power consumption. Figure 3.4.4 shows the measured 65536-point power spectrum for a 280kHz, -4dBFS differential sinusoidal input signal. The third harmonic tone is at -93dBFS. Figure 3.4.5 shows the measured SNR and SNDR versus input amplitude. The peak SNR is 82.4dB and the peak SNDR is 77.6dB. Figure 3.4.6 summarizes the test results. The die micrograph is shown in Fig. 3.4.7. The area of the digital section, including DEM, buffer, and noise cancellation logic is about 30% of the entire active area.

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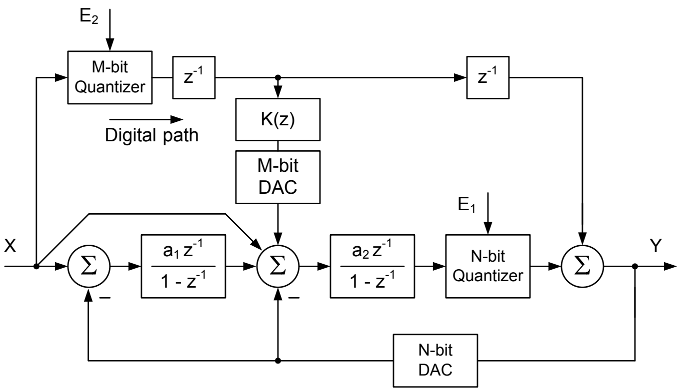

Figure 3.4.1: Block diagram of the ΔΣ modulator.

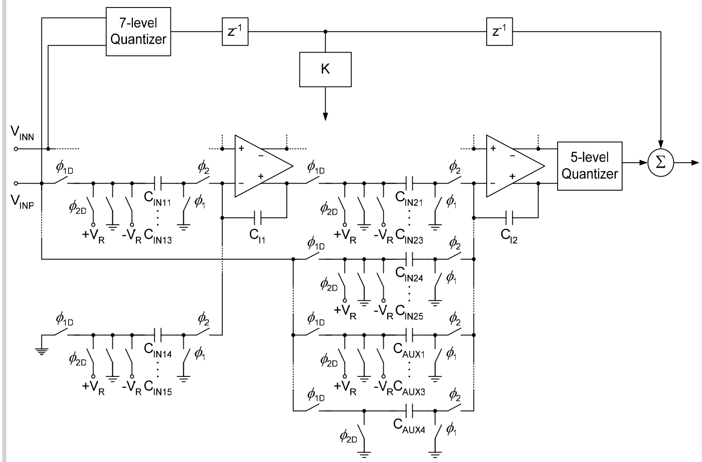

Figure 3.4.2: SC implementation (Only half path).

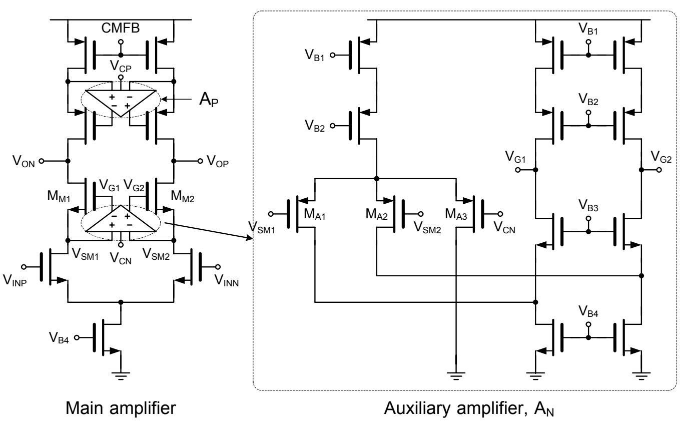

Figure 3.4.3: Gain-boosted OTA for the second integrator.

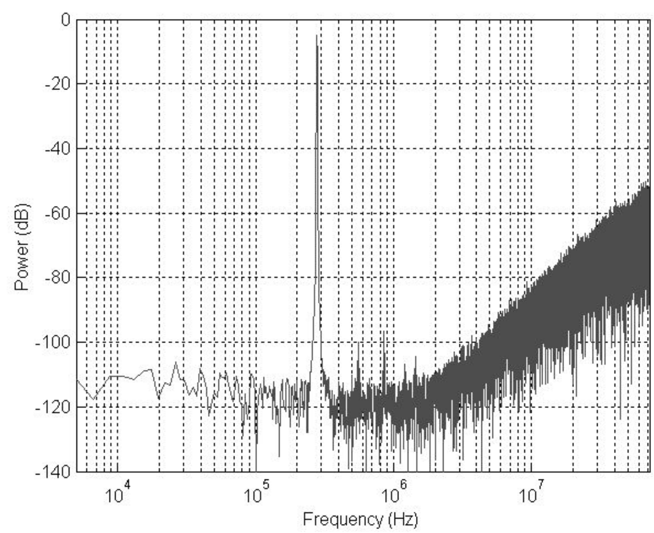

Figure 3.4.4: Output power spectral density.

Sampling frequency	144MHz
Signal bandwidth	2.2MHz
Oversampling ratio	32.7
Peak SNR	82dB (@ V_{IN} = 280kHz)
Peak SNDR	78dB (@ V_{IN} = 280kHz)
Dynamic range	86dB
Input range	$2V_{pp}$ (differential)
Power consumption	5.1mW (A), 8.7mW (D)
Power supply	1.8V (A), 2.5V (D)
Active area	$2.32mm^2$
Technology	0.18µm CMOS

Figure 3.4.5: Performance summary.

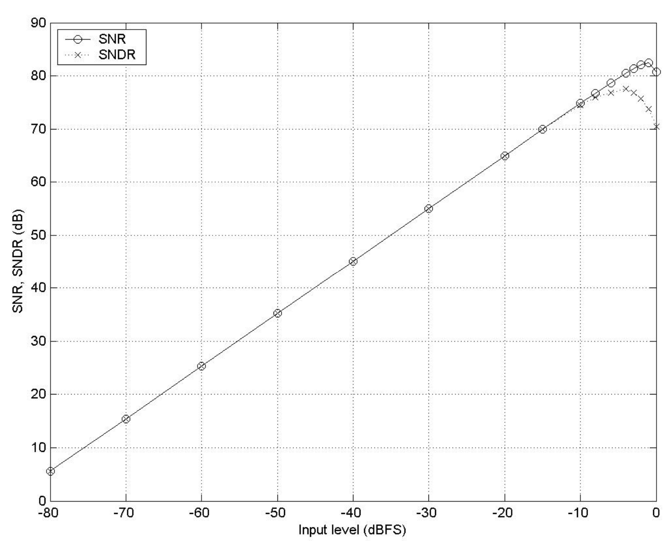

Figure 3.4.6: SNR and SNDR versus input amplitude.

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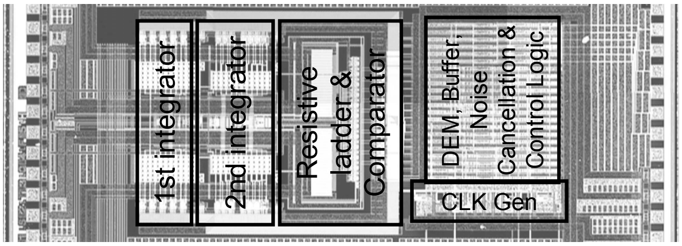

Figure 3.4.7: Die micrograph.